GRAPHENE NANORIBBON BASED CMOS MODELLING

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To my family, especially my beloved wife for her helpful .....to my brother Mahmoud Khudaer Jameil.

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ABSTRACT

Graphene nanoribbons are among the recently discovered carbon nanostructures, with unique characteristics for novel applications. One of the most important features of graphene nanoribbons, from both basic science and application points of view, is their electrical conductivity.The impressive properties of graphene such as the linear energy dispersion relation, room-temperature mobility as high as 15000 $^{cm^2}/_{Vs}$ with current density $2A/mm$ .This is make it an remarkable candidate for electronic devices of the future. Graphene nanoribbon (GNR) with outstanding electrical and thermal properties indicates quantum confinement effect. GNR as a new material which can be used with Si complementary metal oxide semiconductor (CMOS) technology to overcome the integrated circuits hit transfer problems.GNRCMOS devices operated at high source-drain bias show a saturating I-V characteristic. In this project armchair GNR with semiconducting properties in the CMOS technology application is in our focus. Based on the presented model comparison study on transfer characteristic is reported which illustrates that the performance and electrical properties of GNRCMOS.The measurements of the GNRCMOS confirm larger than 0.1 eV bandgap with channel length 20 nm. These parameters have been replicated on CMOS. The low noise margin (NM_L) and the high noise margin (NM_H) are 1.156 and 1.053 volt reported respectively which is comparable by SiCMOS with 0.6744 volt NM_L and 1.39 volt NM_H respectively. The voltage transfer curve (VTC) of GNRCMOS is calculated (13.2978) while for the SiCMOS device is 7.999309.

ABSTRAK

Graphene nanoribon adalah antara nano struktur karbon yang baru dijumpai dan mempunyai ciri-ciri unik bagi penggunaan yang baru. Berdasarkan pengetahuan sains asas, graphene nanoribon dipercayai mampunyai cirri-ciri konduktor elektrik yang sangat baik. Graphene nanoribon mempunyai ciri-ciri yang sangat mengagumkan seperti, tenaga penyebaran yang linear dan pergerakan suhu bilik yang tinggi ($15000cm^2/Vs$) dengan ketumpatan arus sebanyak 2A/mm.Ini menjadikan graphene nanoribon sebagai peranti elektrik yang mempunyai ciri-ciri luar biasa bagi penggunaan masa hadapan.Sifat-sifat elektrik dan terma yang masih belum jelas menunjukkan bahawa terdapat kesan pengurungan kuantum dalam graphene nanoribon (GNR). GNR boleh digunakan sebagai bahan baru di dalam Si teknologi semikonduktor oksida logam pelengkap (CMOS) untuk mengatasi masalah pemindahan dalam litar bersepadu. Peranti GNRCMOS yang beroperasi pada sumber saliran yang tinggi telah menunjukkan ciri-ciri kumpulan I-V. Di dalam projek ini, kami memfokus pada penggunaan GNR untuk diaplikasikan di dalam CMOS teknologi kerana sifatnya sebagai semikonduktor yang baik. Kajian mengenai pernandingan model yang dibentangkan telah menggambarkan prestasi dan sifat elektrik yang baik bagi GNRCMOS. GNRCMOS telah disahkan mempunyai ukuran bandgap yang lebih besar dari 0.1 eV dengan saluran sepanjang 20 nm. Kesemua parameter tersebut telah disalin pada CMOS.NM_L (1.156 volt) dan NM_H (1.053 volt) untuk GNRCMOS telah dibandingkan dengan NM_L (0.6744 volt) dan NM_H (1.39 volt) untuk SiCMOS. Pengiraan keluk pemindahan voltan (VTC) bagi GNRCMOS telah memberikan nilai 13, 2978 manakala untuk peranti SiCMOS adalah 7.999309.

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LIST OF ABBREVIATIONS

SB	–	Schottky Barrier
SEM	–	Scanning Electron Microscope
VTC	–	Voltage Transfer Characteristic
SWNT	–	Single Wall Nanotube
SPINFET	–	Spin Field Effect Transistor
Q1D	–	Quasi-One-Dimensional
Q2D	–	Quasi-Two-Dimensional
PMOS	–	P Channel Metal-Oxide-Semiconductor Swing
NMOS	–	N Channel Metal-Oxide-Semiconductor
PTM	–	Predictive Technology Model
pFET	–	Ptype Field Effect Transistor
SPICE	–	Simulation Program Integrated Circuits Especially
O	–	Ohmic
ND	–	Nondegenerate
nFET	–	Ntype Field Effect Transistor
NEGF	–	Non-Equilibrium Green Function
MWNT	–	Multiwall Nanotube
MOSFET	–	Metal-Oxide-Semiconductor Field-Effect Transistor
MOS	–	Metal-Oxide-Semiconductor
ITRS	–	International Technology Roadmap for Semiconductor
IC	–	Integrated Circuit
HFET	–	Heterojunction Field Effect Transistor
GNR	–	Graphene Nanoribbon

DOS	–	Density of state
DIBL	–	Drain-Induced Barrier Lowering
DC	–	Direct Current
D	–	Degenerate
CVD	–	Chemical Vapour Deposition
CNFET	–	Carbon Nanotube Field-Effect Transistor
CMOS	–	Complementary Metal-Oxide-Semiconductor
CNT	–	Carbon Nanotube
AC	–	Alternative Current
ABM	–	Analog Behavioural Modeling
	–	

LIST OF SYMBOLS

σ	–	Conductivity
γ	–	Fitting parameter
Γ	–	Gamma function
$\Im$	–	Fermi-Dirac function
ψ	–	Wavefunction
V_T	–	Threshold voltage
V_t	–	Thermal voltage
V_{GS}	–	Gate to source voltage
V_{DS}	–	Drain to source voltage
V_{DD}	–	Supply voltage
W	–	Width
V_{ch}	–	Channel voltage
V_c	–	Critical voltage
v_{th}	–	Thermal velocity
v_{sat}	–	Saturation velocity
v_{inj}	–	Injection velocity
v_i	–	Intrinsic velocity
v_f	–	Fermi velocity
v_d	–	Drift velocity
v	–	Carrier velocity
U	–	Potential energy
μ_∞	–	Intrinsic mobility
μ_{eff}	–	Effective mobility

μ_B	–	Ballistic mobility
μ_B	–	Mobility
T	–	Temperature
W	–	Gate oxide thickness
t	–	C-C bonding energy
W	–	Quantum resistance
R_o	–	Ohmic resistance
$R_{channel}$	–	Channel resistance
R_c	–	Contact resistance
R	–	resistance
r	–	Signal resistance
Q	–	Total number of charge
r	–	Signal resistance
q	–	Number of charge
p	–	Momentum
ρ	–	Resistivity
N_c	–	Effective density of state
η	–	Normalized Fermi energy
n	–	Carrier concentration
m^*	–	Effective mass
L_{ind}	–	Inductance
L	–	Length
ℓ_{eff}	–	Effective mean free path
ℓ_B	–	Ballistic mean free path
ℓ	–	Mean free path
k_B	–	Boltzmann Constant
k	–	Wavevector
I_{sat}	–	Saturation current
I_{DS}	–	Drain to source current
h	–	Plank's constant

G	–	Conductance
F	–	Carrier force
E_v	–	Valence band
E_g	–	Bandgap energy
E_F	–	Fermi energy
E	–	energy
ε_o	–	Vacuum permittivity
E_C	–	Conduction band
ε_c	–	Critical electric field
ε	–	Electric field
D_o	–	Metallic density of state
$D(E)$	–	Density of state
d	–	Diameter
C_Q	–	Quantum capacitance
C_C	–	Oxide capacitance
C_L	–	Load capacitance
C_int	–	Intrinsic capacitance
C_{GS}	–	Gate to source capacitance
C_{GD}	–	Gate to drain capacitance
C_g	–	Gate capacitance
C_{ext}	–	Extrinsic capacitance
C_{DB}	–	Drain to bulk capacitance
C	–	Capacitance
A	–	Area cross section
a_{cc}	–	Nearest C-C bonding distance
a	–	Vector of lattice
	–	

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CHAPTER 1

INTRODUCTION

1.1 Research Background

The transistors on a modern Intel Pentium chip are 200 times smaller than 10 millionths of an eter in spite of the prediction by scientists, in 1961, that transistors on a chip could ever be smaller than that [1]. Researchers are currently working on innovative ways of building tiny devices. In particular, several emerging electronic devices such as carbon nanotubes Field Effect Transistors (FETs) [2–4], Si nanowire FETs [2–4], and planar IIIV compound semiconductor (e.g., InSb, InAs) FETs [4] are being investigated. They are all promising potential device candidates for integration onto the silicon platform for enhancing circuit functionality and also for the extension of Moores Law [2]. The channel material could be narrow graphene based in future transistors.

”Physicists Andre K. Geim, and Konstantin S. Novoselov, of the University of Manchester in the U.K., won the 2010 Nobel Prize in Physics for their discovery of graphene, a one-atom thick sheet of carbon atoms, arranged in a honeycomb pattern that boasts of outstanding mechanical and electronic properties”.

The ”idea that a single freestanding sheet of graphene, a one atom thick carbon film that rests on or is suspended from (but is not tightly attached to a support) could be isolated had been investigated since the 1980s when carbon nanotubes and buckeyballs were discovered [2]. By the early part of this decade, researchers had concluded that freestanding graphene could not be isolated after years of trying unsuccessfully to separate graphite into its constituent graphene sheets. Thermodynamics principles predicted that the material would spontaneously roll up into a nanotubes or other curved structure. Yet in 2004, Geim and Novoselov, worked out a surprisingly simple method for exfoliating little chips of graphite by folding adhesive tape against the

crystals and repeatedly peeling apart the tape. The team showed that not only could single sheets of graphene be isolated, but they remain particularly stable at room temperature".

An explosion in graphene research resulted from the "discovery of that rudimentary method for isolating graphene sheets. For advanced computing applications , digital displays [3, 4] and other types of flexible electronics [3–5], and advanced composite materials, it has quickly become a top choice. The possibility of using graphene in device applications in a manner similar to carbon nanotubes has risen due to this".

Recently, "carbon nanotubes (CNTs) have enjoyed a lot of attention in the literature, mostly because of their potential to replace silicon (Si) as the material of choice for the channel of Field Effect Transistor (FET) devices. Electron and whole mobility in CNTs have been measured and predicted to be exceedingly high, to the point where CNT-based transistors can be described as nearly ballistic. No straightforward way exists of patterning even simple CNT-based circuits [3], [4] even when the electronic properties of CNTs are excellent for FET applications. Presently, revolutionary advances in process technology appear to be needed for large-scale integration of CNT devices. Grapheme, being a zero-gap semiconductor [2], cannot be used directly in applications such as field-effect transistors (FETs). However, in addition to the two dimensions (2D) confinement, the graphene electrons can be further confined by forming narrow graphene ribbons [5]".

Mistake Fujita and co-authors originally introduced graphene ribbons as a theoretical model to "examine the edge and nanoscale size effect in graphene [4-6], which are essentially edge-terminated graphene sheets. Even though they offer the possibility of lithographic patterning on silicon carbide (Sic) substrates, potentially solving the major obstacle to large-scale integration, the GNRs are expected to have similar electronic properties to CNTs " [3, 4].

X Wang et al [6]"did one of the first works to demonstrate sub-10 nm width GNRFETs. They achieved such dimensions because they started with GNRs that had been chemically derived at smaller dimensions using the process described in Section 2.1.3.1 instead of patterning GNRs from a planar sheet with e-beam lithography. In this process, exfoliated graphene is dispersed into a chemical solution by significations, creating very small fragments. After that, the solution is applied to a substrate, dried and GNRs identified with atomic force microscopy. These GNRs ranged from

monolayer to trilateral. They were deposited on a silicon dioxide (SiO2) dielectric over a highly doped silicon back gate, and contacted with palladium (Pd) source/drain electrodes". It is a new project referred to as Graphene-based Nan electronics.

With financial support from the European Commission, devices (GRAND) have recently been set up in Europe to investigate technical aspects connected with the feasibility, design, fabrication and complimentary metal-oxide-semiconductor (CMOS) integration of graphene nanoribbon field effect transistors (GNRFETs).

"The semi-classical top-of-the-barrier ballistic model [7] was utilized with the corresponding calculated band-structure", in this study, to investigate the performance of MOSFET like-GNRFET. This model can capture 2D electrostatics based on a simple capacitance model, calibrated to the device structure. Through the self-consistent calculation, it can also capture quantum capacitance. It calculates the carrier transport properties based on the electronic structure of the channel at the top of the barrier. It provides insights of device physics, even though it is a simple model. It has also been widely utilized in investigating the ultimate device performance of the different novel channel MOSFETs.

The upper limit performance potential of ballistic graphene nanoribbon MOSFETs is examined using the "semi-classical top-of-the-barrier ballistic" model In X et al [4]. It has been shown in their study that semiconducting ribbons, that are a few nanometers in width, electronically behave in a manner similar to carbon nanotubes, thus attaining similar on-current performance. The authors compared ideal, ballistic GNR MOSFETs with width w=2.2nm and 4.2nm to an ideal ballistic Si MOSFETs whose device structure was specified by the 90nm node of ITRS report. They found that an ideal ballistic MOSFET can be outperform by an ideal ballistic GNR MOSFET by up to 200 % in terms of on-current density at a fixed off-current.

The device performance of different type of GNR MOSFETs has been evaluated and compared to a cylindrical gate "CNT MOSFETs using the semi-classical top-of-the-barrier ballistic model "in the study by X et al [3]. The 1nm diameter cylindrical CNT MOSFET outperformed the 1.4nm width single gate armchair GNR MOSFET by 200% in terms of on-current density as shown by the study. The 1.4nm width double gate armchair GNR (with similar band gap (0.8eV) as the 1nm diameter zigzag CNT) MOSFET, has, however, performance comparable to the 1nm diameter cylindrical CNT MOSFET. Next, the authors investigated in detail, the ultimate performance of a 3nm width armchair GNR MOSFET with double gate structure.

Compared to the 1nm diameter zigzag CNT, the 3nm wide armchair GNRs has similar width as the circumference of the CNT, but has a smaller band gap (0.5eV). The double gate 3nm width armchair GNR MOSFET was found to have outperformed both the cylindrical 1nm diameter CNT MOSFET and the double gate 1.4nm width armchair GNR MOSFET when the total current and current density were evaluated.

1.2 Production

Single-layer graphene was first produced by a mechanical exfoliation technique. Starting with highly oriented pyrolytic graphite (HOPG), a sticky ”scotch tape was used to peel-off a few layers of graphene”. Since the ”graphite” is sliced into two parts, each part has to be thinner than the original one. Repeating it several times produces thin flakes, which can be transferred to a (silicon) substrate. Single layer flakes can be identified by optical microscopy (Figure 1.2 (left)) [8] and can be verified by Raman measurements [9] or by atomic force microscope (AFM).

A more ”scalable” method to produce graphene is to grow it on a suitable planar surface using ”chemical vapor deposition (CVD), molecular beam epitaxy (MBE), or by ”the reduction of SiC [10–12]. These methods can now produce both multilayer and single-layer graphene on large-area substrates [Figure 1.2 (right)]. The clear advantage is that one can cover an entire wafer with graphene by such growth methods. The CVD technique is often performed on metal substrates (Cu, Ni, Ru) due to the underlying hexagonal symmetry of the lattice, which initiates graphene formation. The low solid solubility of carbon results in limited, few-layer growth [10].

These as-grown thin films on metal cannot be used in ordinary electronic applications due to the direct (electrical) contact with the underlying metal. However, it is possible to transfer the graphene from them to insulating substrates like silicon or quartz by etching the metal substrate away. Epitaxial growth on insulating SiC substrates is also possible. At high temperatures, the surface Si-C atoms start to dissociate, and Si is pumped away, leaving excess carbon on the surface, which reconstruct as a graphene layer [11,13,14]. It has now established that such ’epitaxial-graphene’ layers are identical to graphene obtained by other methods.

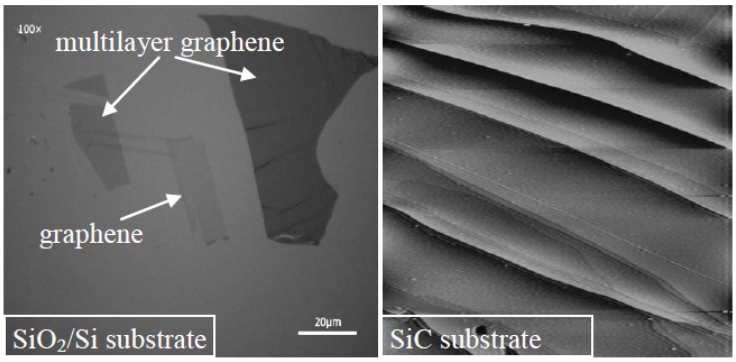

Figure 1.1: (left) Example of an ex foliated graphene flake. There is a monolayer flake on the middle, double layer flake on the left and a multilayer flake on the right. (right) AFM micrograph of the epitaxially grown graphene surface on SiC. The graphene is atomically smooth; the steps are of the substrate. The image is 10 x 10 um, gray scale range: 20 nm.

1.3 Objective

Focus of this study is to evaluate the upper limit performance potential of graphene nanoribbon CMOS and specifically:

(a) Study and analyze the electrical properties of GNR on the CMOS technology.

(b) Understand the electrical characteristics of this low dimension transistor.

(c) Study the possible role of GNRCMOS in future electronic systems.

(d) Improvement of GNR CMOS performance through simulation by using T-spice and MATLAB.

1.4 Problem Statement

Every three years, the progress in device scaling has followed an exponential curve with the doubling of the device density on a microprocessor. This is now known as Moore's law. It was initiated by Intels founder, Gordon Moore. Continued success in device scaling is necessary for maintaining the evolutionary technological improvements that have been the foundation for integrated circuit development and design this far. The channel length of CMOS has pushed by this into the nanoscale regime. With the extreme scaling of CMOS, new challenges arise as the Si based

CMOS reaches its performance limits, with short channel effects coming into place. This brings us to the search of new devices or materials which would be able to keep the transistor scaling in accordance with Moores Law. .

”Yet we do need an adjunct to silicon, because so much of the potential market for electronics has yet to be opened. Electronics in paper, on walls, and in clothing are today mere novelties, simply because silicon can’t easily be painted on a surface, draped on a flexible platform, or used to cover large areas. What’s needed is something that can do all that and still be churned out cheaply and in bulk, processed easily, and slipped deftly into the guts of the next generations of electronics”.

Grapheme, the alternative material, is at the top of the substituent list. There has been many contenders for Silicon ”in the past, these includes germanium (the material used for the very first transistor), and gallium arsenide, which in spite of its usefulness is still a mere niche material. Why do we therefore nurse such high hopes for this rarefied form of carbon” This study seeks to fill the gap by separating reality from hype.

1.5 Scope of the Study

The T-spice and MATLAB used in the simulation of the proposed technique is the base for analysis in this thesis. Therefore we did not considered the experimental details of the resulting device. The production of GNRCMOS is currently at the embryonic stage. The simulation is therefore not based on any existing standard although the current novel transistor and some experimental data on GNRCMOS are considered in selecting simulation parameters. The comparison of study between SiCMOS and GNRCMOS base on analysis voltage transfer characteristic (VTC) and current voltage curve (I-V curve).

1.6 Summary

It is important that ”the potential device candidates that will be integrated onto the silicon platform to enhance circuit functionality and also for extending Moores Law should be frequently benchmarked against the existing and anticipated silicon (Si) analog transistor data”. In this study, we will:

- Try on measurement the progress of research.
- ”Identify the various device-related strengths, as well as limitations of these novel devices and focus on solving these device related problems in order to accelerate the research progress”.
- Study the possible role of GNRCMOS in future electronic systems.
- The Comparison of study via modeling & simulation.

1.7 Organization of project

At the beginning, Chapter 1 shows the introduction on nanodevices, carbon nanotube and graphene nanoribbon and the study on CMOS and FET and application them, then discussing the ”objectives of the project and the scope of the research” taken in consideration the analysis graphene nanoribbon and comparison between SiCMOS and GNRCMOS. After that, to study the solution of how to analysis Voltage Transfer Characteristic VTC from I-V curve and comparison with simulation part for SiCMOS.

While, Chapter 2 clarify the structure and background of graphene nanoribbon. Also study on properties on graphene nanoribbon. And make comparison between carbon nanotube and graphene nanoribbon base on properties. Also in same chapter discussion the challenging in graphene that are surface and interface effects on charge transfer, contact resistance, high k insulator, deposition method, band gap engineering method, mobility, integration , doping and compatibility with CMOS. Moreover Why use graphene in CMOS. In chapter discus desirable electric characteristics which are comparable to that achieved in CNTs, such as the fast switching behaviors, high carrier mobility and ballistic transport which were discussed earlier.

Chapter 3 explains the methodology of this study. Method is find drain current in graphene nanoribbon CMOS (GNRCMOS) and modeling equation by using matlab and T-SPICE.

Chapter four contains the results of different value VGS, VDS and extract the data to draw VTC.Their comparison with simulation part finally chapter five gives the conclusion and future work for this study.

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